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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,607	06/26/2001	Robert A. Abbott	LVPAT021US	8672

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EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	4

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,607	ABBOTT, ROBERT A.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-28* is/are allowed.

6)☒ Claim(s) *1-5,7,8 and 12* is/are rejected.

7)☒ Claim(s) *6,9-11,13-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/26/01 & 2/13/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. Claims 1-28 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 7-8, 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable Imada (US Patent 4,797,886) in view of

Ozawa et al. (US Patent 6,038,649 hereafter referred to as Ozawa).

As per claim 1:

Imada substantially teaches the invention. Imada teaches:

- A method of testing memory [abstract, fig. 4, col. 1, lines 5-9]

comprising:

- executing each instruction [col. 2, lines 37-50] of a plurality of test instructions in sequence [col. 4, lines 56-67 and col. 10, lines 26-31];
- executing in sequence the instructions of the group of instructions with which said each instruction is associated for a predetermined number of repeat cycles for said group [col. 11, lines 18-33];
- modifying predetermined fields of each instruction in accordance with a predetermined field modification instructions for each said repeat cycle [col. 8, lines 34-55].

Imada does not explicitly teach:

- an inactive and active repeat control field.

However Imada does disclose capability of:

- A memory testing [abstract, fig. 4, col. 10, lines 10-15] comprising:

- a connectivity among repeat register, program controller, instructions area, and other computing devices [fig. 4, col. 6, lines 53 through col. 7, lines 67];

- a repeat control means used for releasing signal and suspending of the advancement of program memory addresses [col. 11, lines 18-33];

- a repeat register used for storing operation signals [col. 11, lines 48-50].

In addition, Ozawa explicitly teaches:

- An address generating circuit of simple configuration for repeating a selected block of instruction [abstract, fig. 6, col. 21, lines 53-57] comprising:

- a connectivity among multiplexor, comparator, counter, adder, etc...and other computing devices [fig. 2, col. 6, lines 27-67];

- a repeate execution of the program in memory region [col. 5, lines 1-10];

- an active and inactive control signaling used via program counter [col. 22, lines 1-8].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made first, to realize the Imada's memory testing comprising a repeat control means used for releasing signal and suspending of the advancement of program memory addresses as well as a repeat register used for storing operation signals as being the inactive and active repeat control field as claimed by Applicant. This is because the Imada does apply the repeat control mean in both active and inactive mode within the memory testing in ensuring the memory test execution performing correctly. By utilizing this approach, Imada can enhance the memory instruction testing process within the memory system; second, one would modify the Imada's memory testing to explicitly including the repeat execution of the program in memory region as well as the active and inactive control signaling used via program counter as taught by Ozawa's address generating circuit of simple configuration for repeating a selected block of instruction in supporting the compute memory array testing.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to provide the computer memory testing system with a mechanism to enhance the instruction execution process via repeating cycle, repeating register, repeating controller, etc... capabilities. By utilizing this approach, the computer memory testing can achieve in high performance, availability, and operation. The combination further enhances the computer memory testing in a high reliability and flexibility environment, which will correctly provide optimum data availability and transmission throughput among end user real-time communication and execution.

As per claim 2:

Imada further teaches:

- loading into a first repeat instruction address register, the address of the first instruction in the group of instructions [abstract, col. 11, lines 47-50];

- loading into a repeat cycle register a value indicating the number of repeat cycles to be performed for the group; and [col. 11, lines 48-50];

- loading field modification commands for each repeat cycle into a field modification register associated with said each repeat cycle [col. 11, lines 59-64].

In addition, Ozawa explicitly teaches:

- loading into a first repeat instruction address register, the address of the first instruction in the group of instructions [abstract, col. 5, lines 1-10];
- loading into a repeat cycle register a value indicating the number of repeat cycles to be performed for the group; and [col. 5, lines 11-17];
- loading field modification commands for each repeat cycle into a field modification register associated with said each repeat cycle [col. 5, lines 11-15].

As per claims 3-5:

Imada further teaches:

- modifying the instruction field to a complementary value [col. 2, lines 10-20 and lines 51-67].
- modifying the least significant bit of the instruction field to a complementary value [col. 4, lines 25-38].
- generating modified field modification instructions from the field modification instructions associated with said

first and second groups [col. 20, lines 62 through col. 21, lines 19].

In addition, Ozawa explicitly teaches:

- modifying the instruction field to a complementary value [col. 3, lines 59 through col. 4, lines 11];
- modifying the least significant bit of the instruction field to a complementary value [col. 4, lines 46-67].

As per claims 7:

This method claim 7 is similar to method claims 1-5. The only minor different is that claim 7 combined most of claims 1-5's limitation into one. Therefore, this claim is also rejected under the same rationale applied against claims 1-5. **In addition, all of the limitations have been noted in the rejection as per claims 1-5.**

As per claim 8:

Imada further teaches:

- instructions having a next instructions field containing a one or more conditions fields for determining the next instruction to be executed [col. 8, lines 34-55].

In addition, Ozawa explicitly teaches:

- instructions having a next instructions field containing a one or more conditions fields for determining the next instruction to be executed [col. 1, lines 30-35].

As per claim 12:

Imada substantially teaches the invention. Imada teaches:

- In a memory test controller for testing a memory array [abstract, fig. 4, col. 1, lines 5-9 and col. 5, lines 18-28]

comprising:

- a test instruction register array having registers for storing a plurality of test instruction [col. 4, lines 56-67 and col. 10, lines 26-31];
- each register having instruction fields for storing memory addressing sequencing data [col. 11, lines 18-33];
- write data sequencing data [col. 2, lines 15-20];
- a repeat module for repeating a group of one or more test instructions with modified data [col. 8, lines 34-55].
- storage means for storing instruction field modification data [col. 9, lines 45-55].

Imada does not explicitly teach:

- an instruction field for enabling or disabling said repeat module.

However Imada does disclose capability of:

- A memory testing [abstract, fig. 4, col. 10, lines 10-15] comprising:

- a connectivity among repeat register, program controller, instructions area, and other computing devices [fig. 4, col. 6, lines 53 through col. 7, lines 67];

- a repeat control means used for releasing signal and suspending of the advancement of program memory addresses [col. 11, lines 18-33];

- a repeat register used for storing operation signals [col. 11, lines 48-50].

In addition, Ozawa explicitly teaches:

- An address generating circuit of simple configuration for repeating a selected block of instruction [abstract, fig. 6, col. 21, lines 53-57];

comprising:

- a connectivity among multiplexor, comparator, counter, adder, etc...and other computing devices [fig. 2, col. 6, lines 27-67];

- a repeate execution of the program in memory region [col. 5, lines 1-10];

- an active and inactive control signaling used via program counter [col. 22, lines 1-8].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made first, to realize the Imada's memory testing comprising a repeat control means used for releasing signal and suspending of the advancement of program memory addresses as well as a repeat register used for storing operation signals as being the instruction field for enabling or disabling said repeat module as claimed by Applicant. This is because the Imada does apply the repeat control mean in both enabling or disabling (i.e., active and inactive mode) within the memory testing in ensuring the memory test execution performing correctly. By utilizing this approach, Imada can enhance the memory instruction testing process within the memory system; second, one would modify the Imada's memory testing to explicitly including the repeat execution of the program in memory region as well as the active and inactive control signaling used via program counter as taught by Ozawa's address generating circuit of simple

configuration for repeating a selected block of instruction in supporting the compute memory array testing.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to provide the computer memory testing system with a mechanism to enhance the instruction execution process via repeating cycle, repeating register, repeating controller, etc... capabilities. By utilizing this approach, the computer memory testing can achieve in high performance, availability, and operation. The combination further enhances the computer memory testing in a high reliability and flexibility environment, which will correctly provide optimum data availability and transmission throughput among end user real-time communication and execution.

Allowable Subject Matter

4. Claims 6, 9-11, and 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 17-28 are allowable over the prior art of record.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (703) 305-9408. The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel, can be reached on (703)305-9713. The fax phone number for this Group is (703)746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML
4/5/04